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(54) **THROUGH VIA NUB REVEAL METHOD AND STRUCTURE**

(71) Applicant: **Amkor Technology, Inc.**, Chandler, AZ (US)

(72) Inventors: **Ronald Patrick Huemoeller**, Gilbert, AZ (US); **Frederick Evans Reed**, Raleigh, NC (US); **David Jon Hiner**, Chandler, AZ (US); **Kiwook Lee**, Seoul (KR)

(73) Assignee: **AMKOR TECHNOLOGY, INC.**

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CPC ***H01L 21/78*** (2013.01); ***H05K 3/4038*** (2013.01); ***H05K 3/42*** (2013.01); *Y10T 29/49165* (2015.01); *Y10T 29/49204* (2015.01)

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See application file for complete search history.

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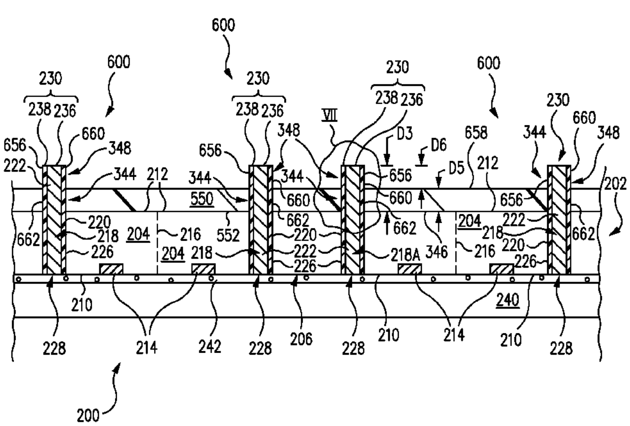
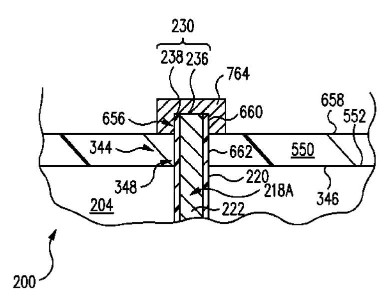
Primary Examiner — Peter DungBa Vo
Assistant Examiner — Kaying Kue
(74) *Attorney, Agent, or Firm* — McAndrews, Held & Malloy, Ltd.

(57) **ABSTRACT**

A method includes applying a backside passivation layer to an inactive surface of an electronic component and to enclose a through via nub protruding from the inactive surface. The method further includes laser ablating the backside passivation layer to reveal a portion of the through via nub. The backside passivation layer is formed of a low cost organic material. Further, by using a laser ablation process, the backside passivation layer is removed in a controlled manner to reveal the portion of the through via nub. Further, by using a laser ablation process, the resulting thickness of the backside passivation layer is set to a desired value in a controlled manner. Further, by using a laser ablation process, the fabrication cost is reduced as compared to the use of chemical mechanical polish.

10 Claims, 6 Drawing Sheets





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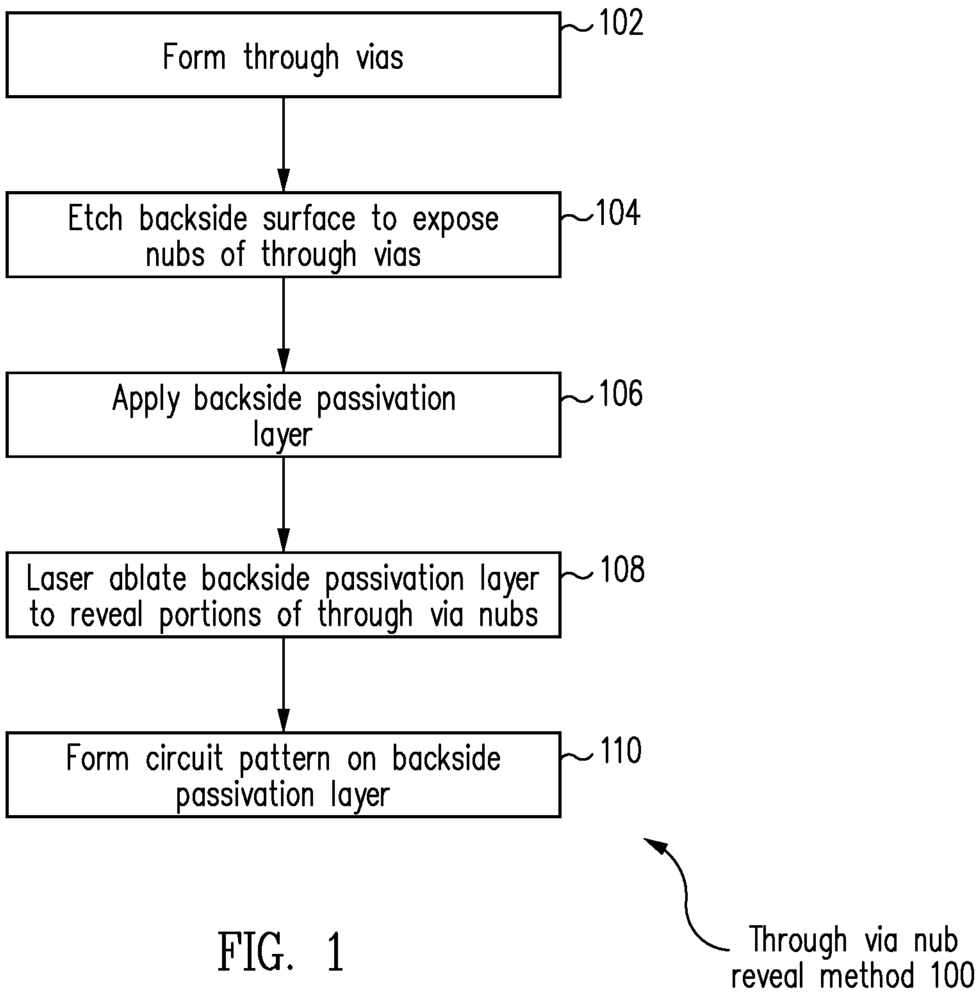

Form through vias
102
Etch backside surface to expose nubs of through vias
104
Apply backside passivation layer
106
Laser ablate backside passivation layer to reveal portions of through via nubs
108
Form circuit pattern on backside passivation layer
110
Through via nub reveal method 100

FIG. 1

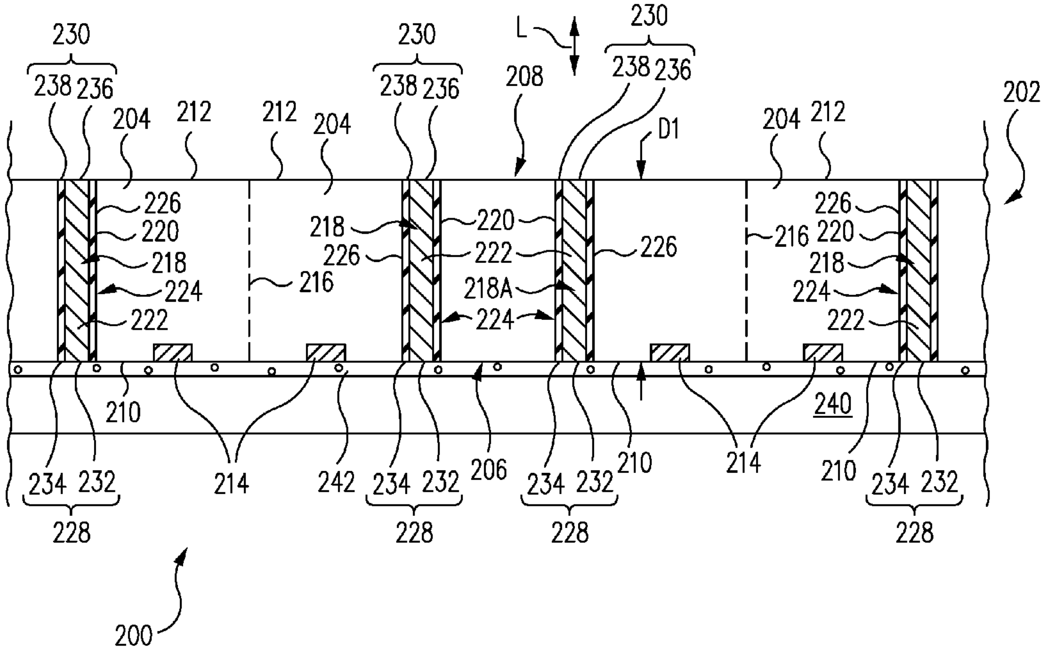

230
238
236
204
212
212
204
230
238
236
L
208
230
238
236
D1
204
212
202
226
220
218
224
222
216
218
226
220
222
218A
224
226
216
226
220
218
224
222
240
210
214
242
206
210
214
210
234
232
228
234
232
228
234
232
228
234
232
228
200

FIG. 2

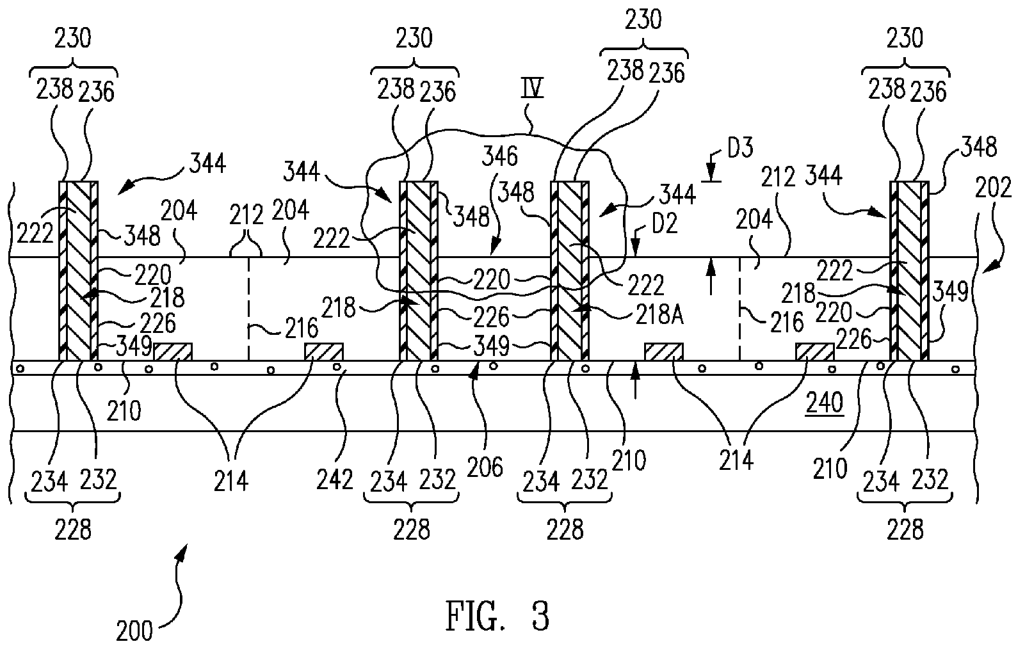

230
238 236
344
222
348
204
212
220
218
226
349
216
IV
346
D3
D2
218A
202
240
210
214
242
206
234 232
228
200

FIG. 3

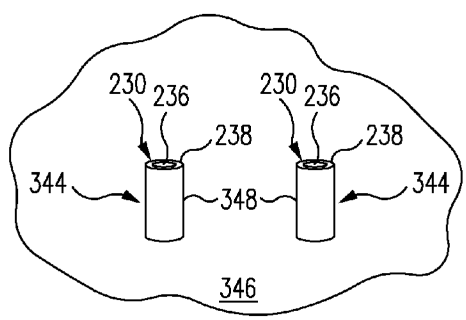
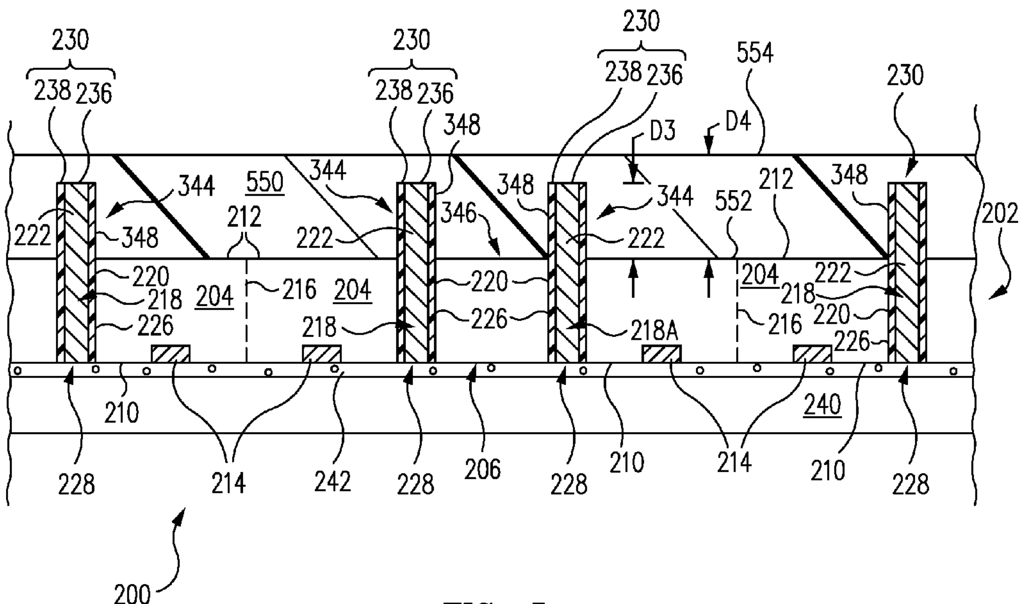

230
236
238
344
348
346

FIG. 4


230
238 236
230
238 236
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238 236
554
230
348
D3
D4
344
550
344
348
344
552
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348
202
222
348
212
222
346
222
222
220
218
204
216
204
220
226
204
218
220
226
226
218
218A
216
226
210
240
228
214
242
228
206
228
210
214
210
228
200

FIG. 5

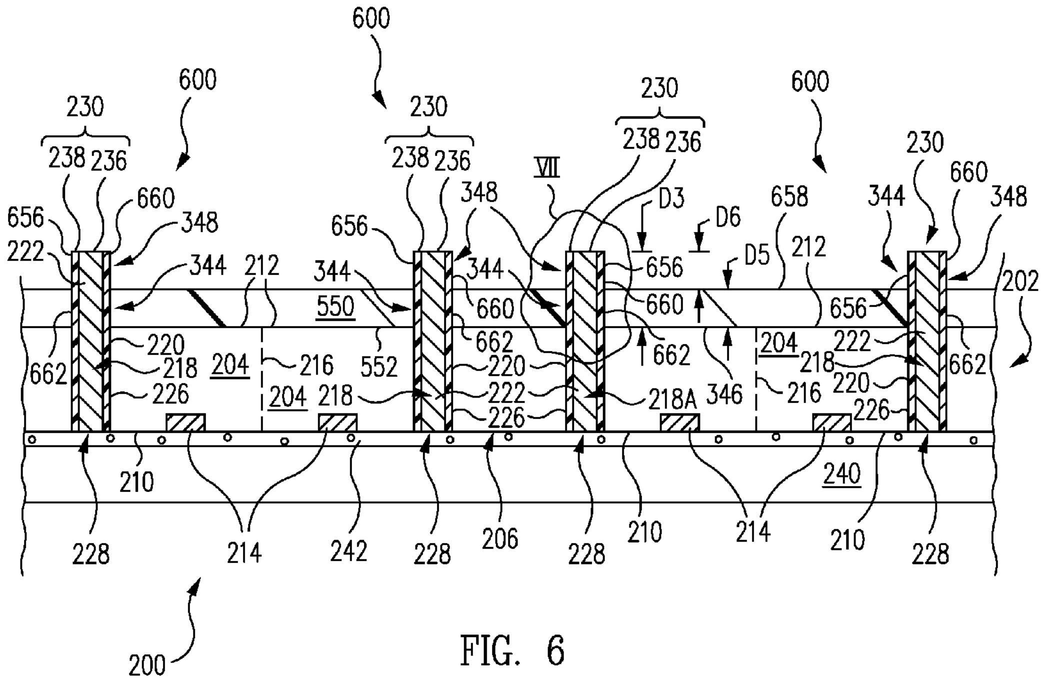

600
600
600
230
238 236
656
222
660
348
344
212
550
552
204
216
218
220
226
662
VII
D3
D6
D5
658
202
346
218A
240
228
210
214
242
206
200

FIG. 6

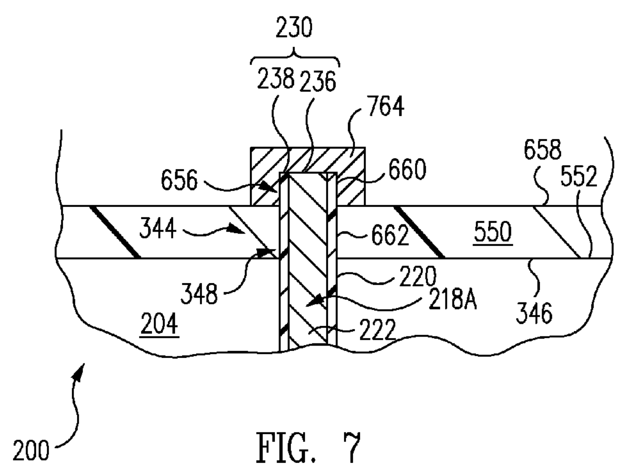
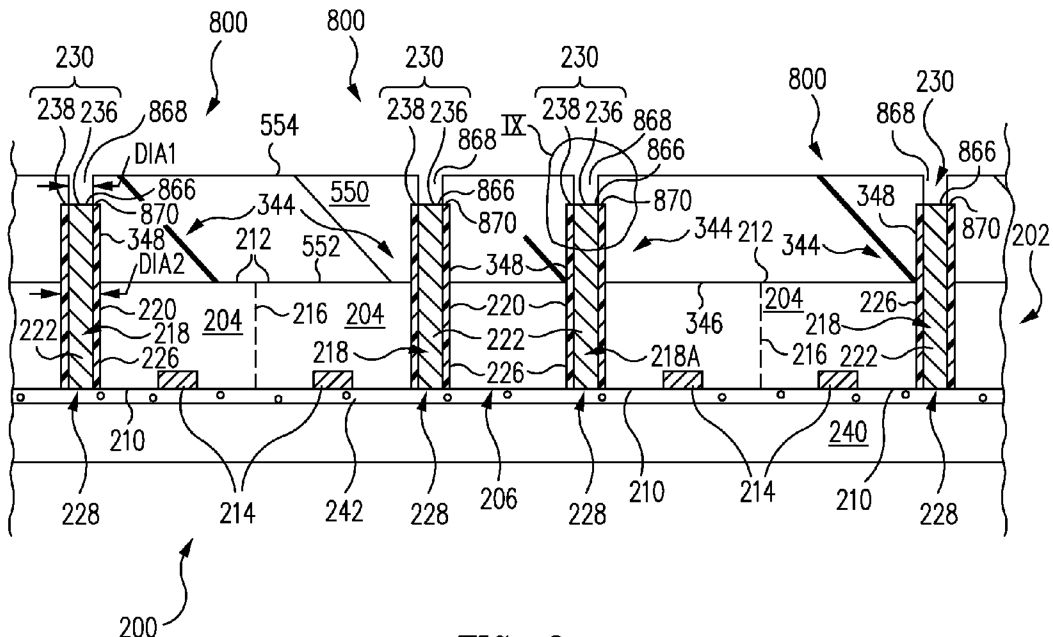
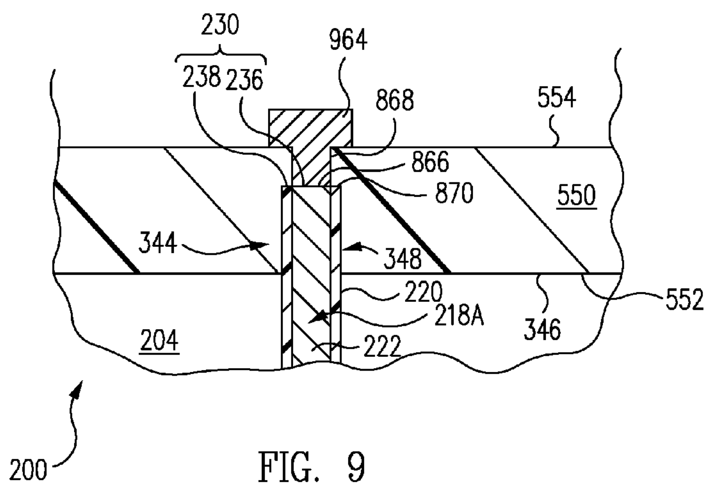

230
238 236
764
656
660
658
552
344
662
550
348
220
218A
204
222
346
200

FIG. 7



800
800
230
238 236
868
DIA1
866
870
554
550
344
348
DIA2
212
552
220
218
222
226
204
216
204
218
238 236
868
866
870
348
220
222
226
IX
230
238 236
868
866
870
344 212
344
218A
800
346
204
216
222
868
230
866
348
870
202
226
218
240
210
228
214
242
228
206
228
210
214
210
228
200

FIG. 8



230
238 236
964
868
554
866
870
550
344
348
220
218A
222
204
346
552
200

FIG. 9

THROUGH VIA NUB REVEAL METHOD AND STRUCTURE

RELATED APPLICATIONS

This application is a divisional of Huemoeller et al., U.S. patent application Ser. No. 12/754,837, filed on Apr. 6, 2010, entitled "THROUGH VIA NUB REVEAL METHOD AND STRUCTURE," which is herein incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present application relates to the field of electronics, and more particularly, to methods of forming electronic component structures.

2. Description of the Related Art

To allow backside contact to an electronic component such as an integrated circuit die, electrically conductive through vias are formed in the electronic component. The through vias extend entirely through the electronic component from the active surface to the inactive surface of electronic component.

The inactive surface of the electronic component is etched to reveal through via nubs, i.e., portions, of the through vias. A chemical vapor deposition (CVD) inorganic dielectric layer such as a plasma enhanced chemical vapor deposition (PECVD) silicon oxide is deposited on the inactive surface of the electronic component and completely encloses the through via nubs. Unfortunately, formation of a CVD inorganic dielectric layer is relatively expensive thus increasing the fabrication cost.

The inorganic dielectric layer is thinned using chemical mechanical polish (CMP) to reveal the ends of the through via nubs. More particularly, the inorganic dielectric layer and a portion of the through via nubs are thinned such that the exposed ends of the through via nubs are parallel to and coplanar with the exterior surface of the inorganic dielectric layer. Unfortunately, chemical mechanical polish is relatively expensive thus increasing the fabrication cost.

SUMMARY OF THE INVENTION

In accordance with one embodiment, a method includes applying a backside passivation layer to an inactive surface of an electronic component and to enclose a through via nub protruding from the inactive surface. The method further includes laser ablating the backside passivation layer to reveal a portion of the through via nub.

In one embodiment, the backside passivation layer is formed of a low cost organic material. By forming the backside passivation layer of an organic material, the fabrication cost is reduced as compared to the formation of a relatively expensive CVD inorganic dielectric layer.

Further, by using a laser ablation process, the backside passivation layer is removed in a controlled manner to reveal the portion of the through via nub. Further, by using a laser ablation process, the resulting thickness of the backside passivation layer is set to a desired value in a controlled manner. Further, by using a laser ablation process, the fabrication cost is reduced as compared to the use of chemical mechanical polish.

These and other features of the present invention will be more readily apparent from the detailed description set forth below taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a through via nub reveal method in accordance with one embodiment;

FIG. **2** is a cross-sectional view of an array including a substrate including a plurality of electronic components in accordance with one embodiment;

FIG. **3** is a cross-sectional view of the array of FIG. **2** at a later stage during fabrication in accordance with one embodiment;

FIG. **4** is a perspective views of the region IV of the array of FIG. **3** in accordance with one embodiment;

FIG. **5** is a cross-sectional view of the array of FIG. **3** at a later stage during fabrication in accordance with one embodiment;

FIG. **6** is a cross-sectional view of the array of FIG. **5** at a later stage during fabrication in accordance with one embodiment;

FIG. **7** is a cross-sectional view of the region VII of the array of FIG. **6** at a later stage during fabrication in accordance with one embodiment;

FIG. **8** is a cross-sectional view of the array of FIG. **5** at a later stage during fabrication in accordance with another embodiment; and

FIG. **9** is a cross-sectional view of the region IX of the array of FIG. **8** at a later stage during fabrication in accordance with one embodiment.

In the following description, the same or similar elements are labeled with the same or similar reference numbers.

DETAILED DESCRIPTION

As an overview and in accordance with one embodiment, referring to FIG. **5**, a backside passivation layer **550** is applied to an inactive surface **212** of an electronic component **204** and to enclose through via nubs **344** protruding from inactive surface **212**. Referring to FIG. **6**, backside passivation layer **550** is laser ablated to reveal top portions **656** of through via nubs **344**.

In one embodiment, backside passivation layer **550** is formed of a low cost organic material. By forming backside passivation layer **550** of an organic material, the fabrication cost is reduced as compared to the formation of a relatively expensive CVD inorganic dielectric layer.

Further, by using a laser ablation process, backside passivation layer **550** is removed in a controlled manner to reveal top portions **656** of through via nubs **344**. Further, by using a laser ablation process, the resulting thickness of backside passivation layer **550** is set to a desired value in a controlled manner. Further, by using a laser ablation process, the fabrication cost is reduced as compared to the use of chemical mechanical polish.

Now in more detail, FIG. **1** is a block diagram of a through via nub reveal method **100** in accordance with one embodiment. FIG. **2** is a cross-sectional view of an array **200** including a substrate **202** including a plurality of electronic components **204** in accordance with one embodiment.

In one embodiment, substrate **202** is a silicon wafer. Substrate **202** includes a frontside, e.g., first, surface **206** and an opposite backside, e.g., second, surface **208**.

Substrate **202** includes electronic components **204** integrally connected to one another. For simplicity, the term substrate **202** shall be used herein and it is to be understood that this term generally includes electronic components **204**.

In one embodiment, electronic components **204** are integrated circuit chips, e.g., active components. However, in other embodiments, electronic components **204** are passive components such as capacitors, resistors, or inductors.

In accordance with this embodiment, electronic components **204** include active surfaces **210** and opposite inactive surfaces **212**. Active surfaces **210** and inactive surfaces **212** generally define frontside surface **206** and backside surface **208** of substrate **202**, respectively. For simplicity, the terms frontside surface **206** and backside surface **208** shall be used herein and it is to be understood that these terms generally include active surfaces **210** and inactive surfaces **212**, respectively. Electronic components **204** further includes bond pads **214** formed on active surfaces **210**.

Electronic components **204** are delineated from one another by singulation streets **216**. Substrate **202** is singulated, e.g., sawed, along singulation streets **216** to separate electronic components **204** from one another at a later stage during fabrication.

Referring now to FIGS. **1** and **2**, in a form through vias operation **102**, through vias **218** are formed though electronic components **104**. Through vias **218** include dielectric through via passivation linings **220** and electrically conductive through via columns **222**.

Illustratively, through via apertures **224** are formed, e.g., by laser drilling, into electronic components **104** from frontside surface **206**. Through via passivation linings **220**, e.g., silicon oxide (SiO_2), are formed on the sidewalls of through via apertures **224**. In one embodiment, the silicon of substrate **202** exposed within through via apertures **224** is oxidized to form through via passivation linings **220**. In another embodiment, a dielectric material is deposited within through via apertures **224** to form through via passivation linings **220**. In one embodiment, through via passivation linings **220** are 0.15 μm thick although have other values in other embodiments.

Through via columns **222** are formed within through via passivation linings **220**. Illustratively, an electrically conductive material, e.g., copper or tungsten, is deposited, e.g., plated, within through via passivation linings **220** to form through via columns **222**. Through via passivation linings **220** electrically isolate through via columns **222** from substrate **202**.

Substrate **202** is then thinned, sometimes called backgrinded, to expose through vias **218** at backside surface **208** of substrate **202**. In one embodiment, the pitch of through vias **218** is in the range of 10 μm to 30 μm although the pitch has other values in other embodiments.

Through via passivation linings **220** are hollow cylinders and through via columns **222** are solid cylinders formed within through via passivation linings **220**.

Through vias **218** are cylindrical in shape although may taper slightly between frontside surface **206** and backside surface **208**. More particularly, referring to a first through via **218**A of the plurality of through vias **218**, through via **218**A include a cylindrical outer surface **226**, a circular active surface end **228**, and a circular inactive surface end **230**.

Cylindrical outer surface **226** is defined by the cylindrical outer surface of through via passivation lining **220** of through via **218**A. Cylindrical outer surface **226** has a longitudinal axis L perpendicular to frontside surface **206** and backside surface **208**. Cylindrical outer surface **226** extends from active surface end **228** to inactive surface end **230**. Although the terms parallel, perpendicular, and similar terms are used herein to describe various features, in light of this disclosure, those of skill in the art will understand that the features may not be exactly parallel or perpendicular but only substantially parallel or perpendicular to within accepted manufacturing tolerances.

Active surface end **228** is circular in accordance with this embodiment. Active surface end **228** is coplanar with and parallel to frontside surface **206** of substrate **202**.

Active surface end **228** includes a circular active surface column end **232** surrounded by an annular active surface passivation lining end **234**. Active surface column end **232** is the lower end of through via column **222** and thus is electrically conductive. Active surface passivation lining end **234** is the lower end of through via passivation lining **220** and thus is a dielectric.

Similarly, inactive surface end **230** is circular in accordance with this embodiment. Inactive surface end **230** is coplanar with and parallel to backside surface **208** of substrate **202**.

Inactive surface end **230** includes a circular inactive surface column end **236** surrounded by an annular inactive surface passivation lining end **238**. Inactive surface column end **236** is the upper end of through via column **222** and thus is electrically conductive. Inactive surface passivation lining end **238** is the upper end of through via passivation lining **220** and thus is a dielectric.

Although only a single through via **218**A is described in detail, in light of this disclosure, those of skill in the art will understand that all of the through vias **218** include cylindrical outer surfaces **226**, active surface ends **228**, inactive surface ends **230**, active surface column ends **232**, active surface passivation lining ends **234**, inactive surface column ends **236**, and inactive surface passivation lining ends **238** in a similar manner.

As illustrated in FIG. **2**, frontside surface **206** of substrate **202** is mounted to a carrier **240**, e.g., a silicon carrier, by an adhesive **242**. In one embodiment, the thickness of carrier **240** is 700 μm although has other values in other embodiments.

FIG. **3** is a cross-sectional view of array **200** of FIG. **2** at a later stage during fabrication in accordance with one embodiment. FIG. **4** is a perspective views of the region IV of array **200** of FIG. **3** in accordance with one embodiment. Referring now to FIGS. **1**, **2**, **3**, and **4** together, from form through vias operation **102**, flow moves to an etch backside surface to expose nubs of through vias operation **104**.

In etch backside surface to expose nubs of through vias operation **104**, backside surface **208** of substrate **202** is blanket etched, i.e., removed, to expose through via nubs **344** of through vias **218**. In one embodiment, backside surface **208** is removed using a selective etch that etches substrate **202**, e.g., silicon, but does not etch through vias **218**, e.g., silicon oxide and copper.

Generally, in etch backside surface to expose nubs of through vias operation **104**, substrate **202** is thinned from backside surface **208**. Stated another way, a portion of substrate **202** at backside surface **208** as illustrated in FIG. **2** is removed to form a recessed backside surface **346** as illustrated in FIG. **3**.

Accordingly, after performance of etch backside surface to expose nubs of through vias operation **104**, substrate **102** includes a recessed backside surface **346**. Inactive surfaces **212** generally define recessed backside surface **346**. For simplicity, the term recessed backside surface **346** shall be used herein and it is to be understood that this term generally include inactive surfaces **212**.

The distance D2 between recessed backside surface **346** and frontside surface **206** as illustrated in FIG. **3** is less than the distance D1 between backside surface **208** and frontside surface **206** as illustrated in FIG. **2**. Stated another way, substrate **202** is thinned from an initial thickness equal to distance D1 (FIG. **2**) to a final thickness equal to distance D2 (FIG. **3**).

In one embodiment, distance D1 is 50 μm and distance D2 is 48 μm although distances D1, D2 have other values in other embodiments.

However, through vias **218** are not thinned and thus through via nubs **344** are exposed as illustrated in FIG. **3**. Through vias **218** are sometimes said to stand proud of recessed backside surface **346**.

Through via nubs **344** are the upper portions of through vias **218** including the upper portions of through via passivation linings **220** and through via columns **222** exposed and uncovered by substrate **202**. Through via nubs **344** are cylindrical protrusions protruding upwards from recessed backside surface **346**.

Referring again to through via **218**A, through via nub **344** includes a cylindrical nub outer surface **348** and inactive surface end **230**. Cylindrical nub outer surface **348** is the upper, e.g., first, portion of cylindrical outer surface **226** of through via **218**A exposed from substrate **202**. A cylindrical enclosed, e.g., second, portion **349** of cylindrical outer surface **226** of through via **218**A remains enclosed within and in contact with substrate **202**.

Inactive surface end **230** is spaced above recessed backside surface **346**. More particularly, a distance D3 exists between inactive surface end **230** and recessed backside surface **346**. Distance D3 is equal to the difference between the initial thickness (distance D1 as illustrated in FIG. **2**) of substrate **202** prior to performance of etch backside surface to expose nubs of through vias operation **104** and the final thickness (distance D2) of substrate **202** after performance of etch backside surface to expose nubs of through vias operation **104**, i.e., D3=D1−D2. In one embodiment, distance D3 is 2 μm although distance D3 has other values in other embodiments.

Although only a single through via **218**A is described in detail, in light of this disclosure, those of skill in the art will understand that all of the through vias **218** include through via nubs **344** including cylindrical nub outer surfaces **348** in a similar manner.

FIG. **5** is a cross-sectional view of array **200** of FIG. **3** at a later stage during fabrication in accordance with one embodiment. Referring now to FIGS. **1** and **5** together, from etch backside surface to expose nubs of through vias operation **104**, flow moves to an apply backside passivation layer operation **106**. In apply backside passivation layer operation **106**, a backside passivation layer **550** is applied to recessed backside surface **346** of substrate **202** and through via nubs **344**.

Backside passivation layer **550** includes a lower, e.g., first, passivation layer surface **552** attached to recessed backside surface **346**. Backside passivation layer **550** further includes an opposite upper, e.g., second, passivation layer surface **554**, which is planar. Backside passivation layer **550** is a dielectric material.

In one embodiment, backside passivation layer **550** is formed from an organic material such as polyimide (PI), polybutyloxide (PBO), benzocyclobutene (BCB), a polymer, or other carbon containing material. By forming backside passivation layer **550** of an organic material, the fabrication cost is reduced as compared to the formation of a relatively expensive CVD inorganic dielectric layer. In one embodiment, backside passivation layer **550** is formed by spinning or spraying an organic material onto recessed backside surface **346**.

Backside passivation layer **550** has a thickness equal to a distance D**4** between lower passivation layer surface **552** and upper passivation layer surface **554**. In one embodiment, distance D**4** is in the range of 3 μm to 4 μm with a thickness control of ±0.1 μm although distance D**4** has other values in other embodiments.

Distance D**4** is greater than the distance D3 that through via nubs **344** protrude above recessed backside surface **346**. Accordingly, through via nubs **344** including cylindrical nub outer surface **348** and inactive surface ends **230** are completely enclosed within backside passivation layer **550**. More particularly, backside passivation layer **550** exists between inactive surface ends **230** of through vias **218** and upper passivation layer surface **554**.

FIG. **6** is a cross-sectional view of array **200** of FIG. **5** at a later stage during fabrication in accordance with one embodiment. Referring now to FIGS. **1**, **5**, and **6** together, from apply backside passivation layer operation **106**, flow moves to a laser ablate backside passivation layer to reveal portions of through via nubs operation **108**. In laser ablate backside passivation layer to reveal portions of through via nubs operation **108**, backside passivation layer **550** is laser ablated to reveal top, e.g., first, portions **656** of through via nubs **344**.

In accordance with this embodiment, a laser, e.g., an excimer laser, is directed at upper passivation layer surface **554** of backside passivation layer **550**. This laser laser-ablates, i.e., removes, upper passivation layer surface **554** to expose top portions **656** of through via nubs **344** of through vias **218**. Upper passivation layer surface **554** is laser-ablated, sometimes call global or mass ablated, while through via nubs **344** are not removed.

In one embodiment, the laser used during the laser ablation process selectively laser-ablates backside passivation layer **550** and does not laser ablate through via nubs **344** even though the laser is directed at through via nubs **344**. In another embodiment, the laser used during the laser ablation process is directed only at backside passivation layer **550** to avoid laser ablation of through via nubs **344**.

Generally, in laser ablate backside passivation layer to reveal portions of through via nubs operation **108**, backside passivation layer **550** is thinned from upper passivation layer surface **554**. Stated another way, a portion of backside passivation layer **550** at upper passivation layer surface **554** as illustrated in FIG. **5** is removed to form a recessed upper passivation layer surface **658** as illustrated in FIG. **6**.

Accordingly, after performance of laser ablate backside passivation layer to reveal portions of through via nubs operation **108**, backside passivation layer **550** includes a recessed upper passivation layer surface **658**. The distance D4 between upper passivation layer surface **554** and lower passivation layer surface **552** as illustrated in FIG. **5** is greater than the distance D**5** between recessed upper passivation layer surface **658** and lower passivation layer surface **552** as illustrated in FIG. **6**. Stated another way, backside passivation layer **550** is thinned from an initial thickness equal to distance D**4** (FIG. **5**) to a final thickness equal to distance D**5** (FIG. **6**).

However, through vias **218** are not thinned and top portions **656** of through via nubs **344** are exposed. Top portions **656** of through via nubs **344** are the upper portions of through via nubs **344** including the upper portions of through via passivation linings **220** and through via columns **222** exposed and uncovered by backside passivation layer **550**. Top portions **656** of through via nubs **344** are cylindrical protrusions protruding upwards from recessed upper passivation layer surface **658**.

Referring again to through via **218**A, top portion **656** of through via nub **344** of through via **218**A includes a cylindrical top portion outer surface **660** and inactive surface end **230**. Cylindrical top portion outer surface **660** is the upper, e.g., first, portion of cylindrical nub outer surface **348** of through via nub **344** of through via **218**A exposed from backside passivation layer **550**. A cylindrical enclosed, e.g., second, portion **662** of cylindrical nub outer surface **348** of through via nub **344** of through via **218**A remains enclosed within and in contact with backside passivation layer **550**.

Inactive surface end **230** is spaced above recessed upper passivation layer surface **658**. More particularly, a distance D**6** exists between inactive surface end **230** and recessed upper passivation layer surface **658**. Distance D**6** is equal to the difference between the distance D**3** which through via nubs **344** protrude above lower passivation layer surface **552** and distance D**5** between lower passivation layer surface **552** and recessed upper passivation layer surface **658**, i.e., D**6**=D**3**−D**5**.

Although only a single through via **218**A is described in detail, in light of this disclosure, those of skill in the art will understand that all of the through vias **218** include top portions **656**, cylindrical top portion outer surfaces **660** and cylindrical enclosed portions **662** in a similar manner.

By using a laser ablation process, backside passivation layer **550** is removed in a controlled manner around top portions **656** of through via nubs **344**. Further, by using a laser ablation process, the resulting thickness (equal to distance D**5**) of backside passivation layer **550** is set to a desired value in a controlled manner, e.g., to within +0.1 μm. Further, by using a laser ablation process, the fabrication cost is reduced as compared to the use of chemical mechanical polish.

In one embodiment, any residue on recessed upper passivation layer surface **658** and top portions **656** of through via nubs **344** is removed, e.g., using a soft etch, plasma clean, or combination of these techniques.

FIG. **7** is a cross-sectional view of the region VII of array **200** of FIG. **6** at a later stage during fabrication in accordance with one embodiment. Referring now to FIGS. **1** and **7** together, from laser ablate backside passivation layer to reveal portions of through via nubs operation **108**, flow moves to a form circuit pattern on backside passivation layer operation **110**.

In form circuit pattern on backside passivation layer operation **110**, an electrically conductive circuit pattern **764** is formed on backside passivation layer **550**. More particularly, circuit pattern **764** is formed on recessed upper passivation layer surface **658** of backside passivation layer **550**. Backside passivation layer **550** electrically isolates circuit pattern **764** from substrate **202**, i.e., from recessed backside surface **346**.

Circuit pattern **764** is electrically connected to through vias **218**. More particularly, circuit pattern **764** contacts and is electrically connected to inactive surface column ends **236** of through via columns **222** of through vias **218**. As top portions **656** of through via nubs **344** protrude above recessed upper passivation layer surface **658**, electrical interconnection between circuit pattern **764** and through vias **218** is facilitated.

In one embodiment, circuit pattern **764** includes terminals and/or traces. Illustratively, a terminal, sometimes called pad, provides an electrically conductive area to which other electrical conductors, e.g., solder balls, are mounted. A trace is a long yet narrow electrical conductor extending in a horizontal direction substantially parallel to recessed upper passivation layer surface **658** that electrically interconnects other electrical conductors, e.g., terminals of circuit pattern **764**, with one another. Although terminals and traces are set forth as examples of features of circuit pattern **764**, in light of this disclosure, those of skill in the art will understand that circuit pattern **764** is formed with other electrically conductive features in other embodiments depending upon the particular application.

FIG. **8** is a cross-sectional view of array **200** of FIG. **5** at a later stage during fabrication in accordance with another embodiment. Referring now to FIGS. **1**, **5**, and **8** together, from apply backside passivation layer operation **106**, flow moves to laser ablate backside passivation layer to reveal portions of through via nubs operation **108**. In laser ablate backside passivation layer to reveal portions of through via nubs operation **108**, backside passivation layer **550** is laser ablated to reveal contact area, e.g., first, portions **866** of inactive surface ends **230** of through via nubs **344**.

In accordance with this embodiment, a laser is directed at upper passivation layer surface **554** of backside passivation layer **550**. This laser laser-ablates, i.e., removes, selective portions of upper passivation layer surface **554** to reveal contact area portions **866** of inactive surface ends **230** of through via nubs **344** of through vias **218**. Upper passivation layer surface **554** is laser-ablated, i.e., removed, while through via nubs **344** are not removed.

Generally, in laser ablate backside passivation layer to reveal portions of through via nubs operation **108**, circuit pattern apertures **868** are formed in backside passivation layer **550** to expose contact area portions **866** of inactive surface ends **230** of through via nubs **344** of through vias **218**. Circuit pattern apertures **868** extend between upper passivation layer surface **554** and contact area portions **866**. Circuit pattern apertures **868** have a diameter DIA**1** less than a diameter DIA**2** of through vias **218**. In one embodiment, diameter DIA**2** of through vias **218** is less than or equal to 20 μm, e.g., is in the range of 5 μm to 10 μm, although diameter DIA**2** has other values in other embodiments.

Accordingly, contact area portions **866** of inactive surface ends **230** are the portions of inactive surface ends **230** exposed and uncovered by circuit pattern apertures **868**. Further, enclosed area, e.g., second, portions **870** of inactive surface ends **230** of through via nubs **344** of through vias **218** remain enclosed within and covered by backside passivation layer **550**.

In one embodiment, contact area portions **866** are inactive surface column ends **236** of through via columns **222** of through vias **218**. The accordance of this embodiment, enclosed area portions **870** are inactive surface passivation lining ends **238** of through via passivation linings **220** of through vias **218**.

In light of this disclosure, those of skill in the art will understand that in various embodiments a contact area portion **866** includes (1) a portion of inactive surface column end **236** only; (2) the entire inactive surface column end **236**; (3) the entire inactive surface column end **236** and a portion of inactive surface passivation lining end **238**; or (4) a portion of inactive surface column end **236** and a portion of inactive surface passivation lining end **238**, depending upon the diameter of the circuit pattern aperture **868** and the tolerance in alignment of the circuit pattern aperture **868** with the through via **218**.

By using a laser ablation process, circuit pattern apertures **868** are formed in backside passivation layer **550** in a controlled manner to expose contact area portions **866** of through via nubs **344**. Further, by using a laser ablation process, the fabrication cost is reduced as compared to the use of chemical mechanical polish.

FIG. **9** is a cross-sectional view of the region IX of array **200** of FIG. **8** at a later stage during fabrication in accordance with one embodiment. Referring now to FIGS. **1** and **8** together, from laser ablate backside passivation layer to reveal portions of through via nubs operation **108**, flow moves to form circuit pattern on backside passivation layer operation **110**.

In form circuit pattern on backside passivation layer operation **110**, an electrically conductive circuit pattern **964** is formed on backside passivation layer **550**. More particularly, circuit pattern **964** is formed on upper passivation layer surface **554** and within circuit pattern apertures **868** of backside passivation layer **550**. Backside passivation layer **550** electrically isolates circuit pattern **964** from substrate **202**, i.e., from recessed backside surface **346**.

Circuit pattern **964** is electrically connected to through vias **218**. More particularly, circuit pattern **964** contacts and is electrically connected to contact area portions **866** of through vias **218**.

In one embodiment, circuit pattern **964** includes terminals and/or traces in a manner similar to that described above regarding circuit pattern **764** of FIG. **7** and so is not repeated here.

Referring again to FIGS. **6** and **8**, array **200** is singulated on singulation streets **216** to form a plurality of individual electronic component packages **600**, **800**, respectively. More particularly, substrate **202** and backside passivation layer **550** are cut, e.g., using a laser, mechanical sawing, or other singulation technique to form electronic component packages **600**, **800**. However, in other embodiments, array **200** is singulated at later stages during manufacture.

Although formation of a plurality of electronic component packages **600**, **800** simultaneously in array **200** is described above, in other embodiments, electronic component **204** are processed individually (after singulation of substrate **202**) using the methods as described above.

The drawings and the forgoing description gave examples of the present invention. The scope of the present invention, however, is by no means limited by these specific examples. Numerous variations, whether explicitly given in the specification or not, such as differences in structure, dimension, and use of material, are possible. The scope of the invention is at least as broad as given by the following claims.

What is claimed is:

1. A method of manufacturing an electronic component having at least one through via nub, the method comprising:

forming a through via that extends through a semiconductor die, where the semiconductor die comprises an active surface and an inactive surface;

filling the through via with conductive material;

etching the inactive surface of the semiconductor die to expose a through via nub of the conductive material protruding from the inactive surface;

after said etching, applying a backside passivation layer to the inactive surface of the semiconductor die and thereby enclosing the protruding through via nub; and

ablating the backside passivation layer thereby revealing a portion of the through via nub.

2. A method of manufacturing an electronic component having at least one through via nub, the method comprising:

applying a backside passivation layer to an inactive surface of a semiconductor die that comprises the inactive surface and an active surface opposite the inactive surface, wherein the backside passivation layer has a first thickness greater than a distance that a through via nub protrudes from the inactive surface; and

thinning the backside passivation layer to a second thickness less than the distance that the through via nub protrudes from the inactive surface.

3. The method of claim **2** wherein the applying comprises applying the backside passivation layer to the inactive surface and to the through via nub, such that the backside passivation layer completely encloses the through via nub.

4. The method of claim **2** wherein said thinning the backside passivation layer to a second thickness comprises thinning the entire backside passivation layer.

5. The method of claim **2**, comprising after at least said thinning, singulating the semiconductor die from a wafer.

6. The method of claim **2** wherein:

the through via nub comprises a top surface and a cylindrical side surface that protrude from the inactive surface of the semiconductor die; and

after said thinning, a first portion of the cylindrical side surface is covered by the backside passivation layer and a second portion of the cylindrical side surface is exposed from the backside passivation layer.

7. The method of claim **4**, wherein said thinning comprises laser ablating the backside passivation layer.

8. The method of claim **5** wherein said laser ablating comprises directing a laser at the backside passivation layer and the through via nub, the laser selectively laser ablating the backside passivation layer and not the through via nub.

9. The method of claim **5** wherein said laser ablating comprises directing a laser at the backside passivation layer, but not at the through via nub.

10. The method of claim **2**, wherein the backside passivation layer is organic.

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